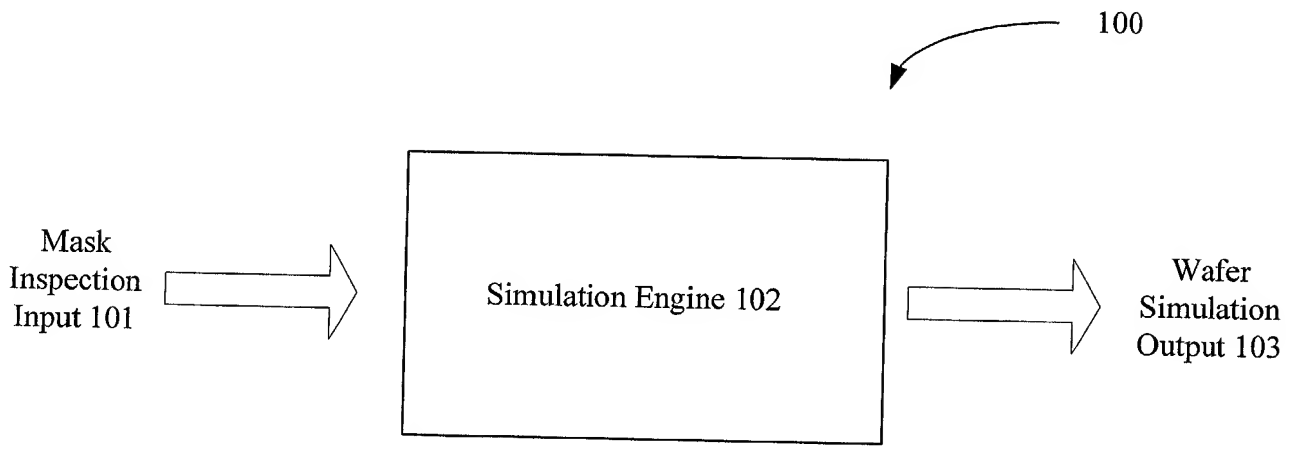
100
Mask
Inspection
Input 101
Simulation Engine 102
Wafer
Simulation
Output 103

Figure 1

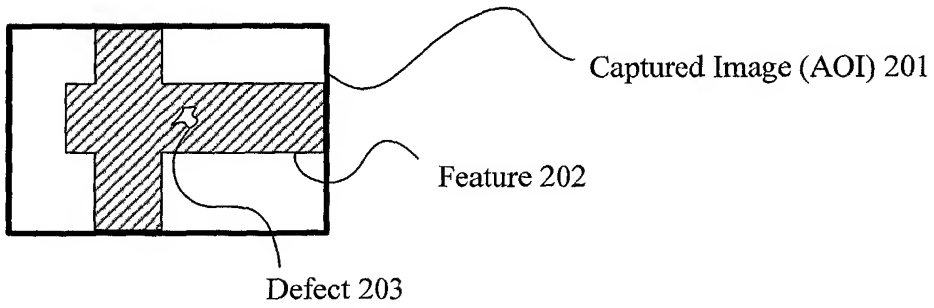

Figure 2A

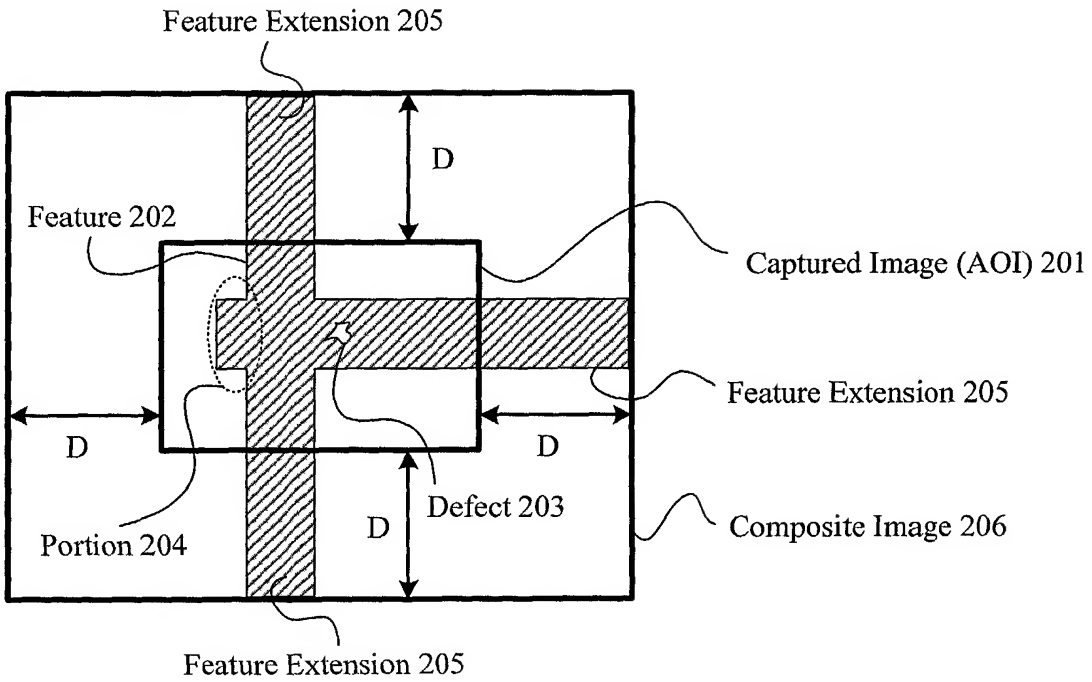

Figure 2B

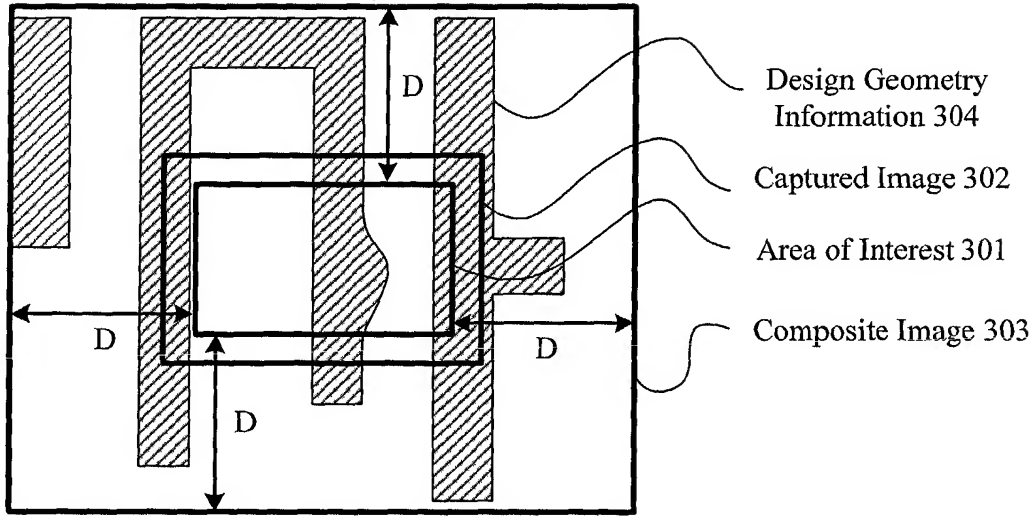

Figure 3A

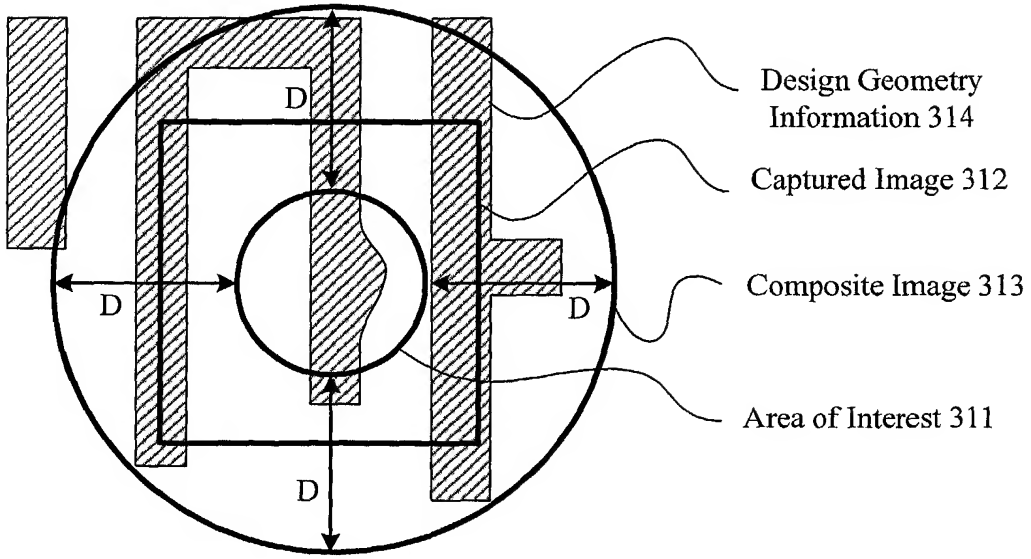

Figure 3B

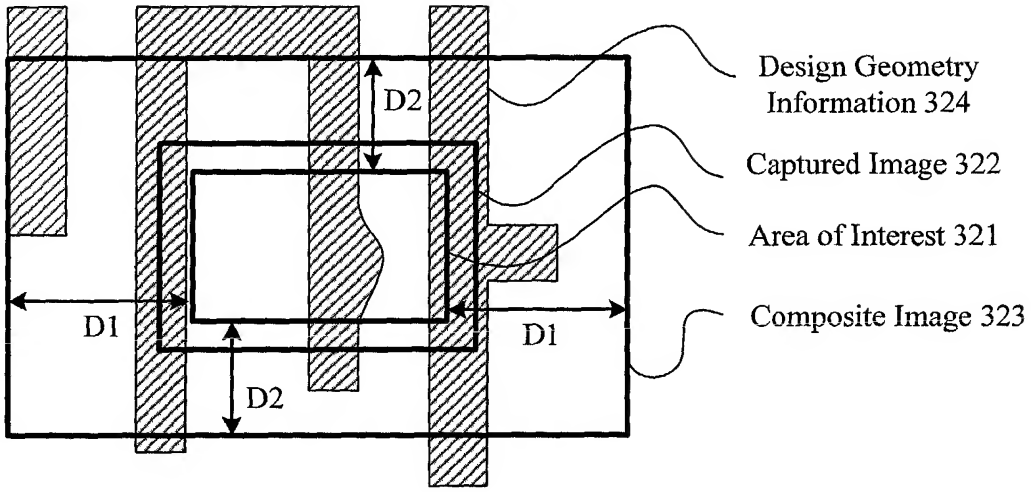

Figure 3C

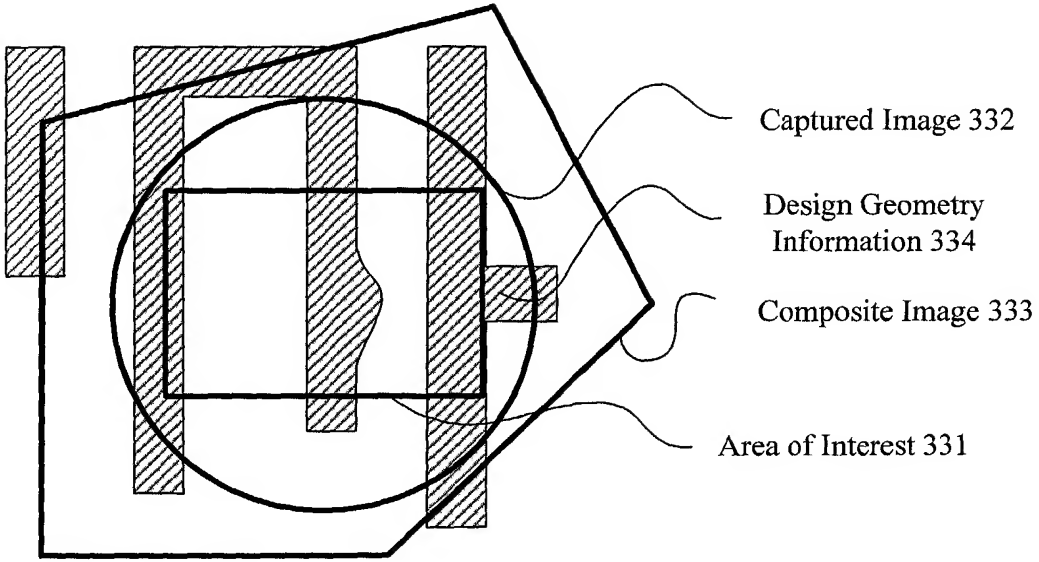

Figure 3D

PATENT DOCUMENT

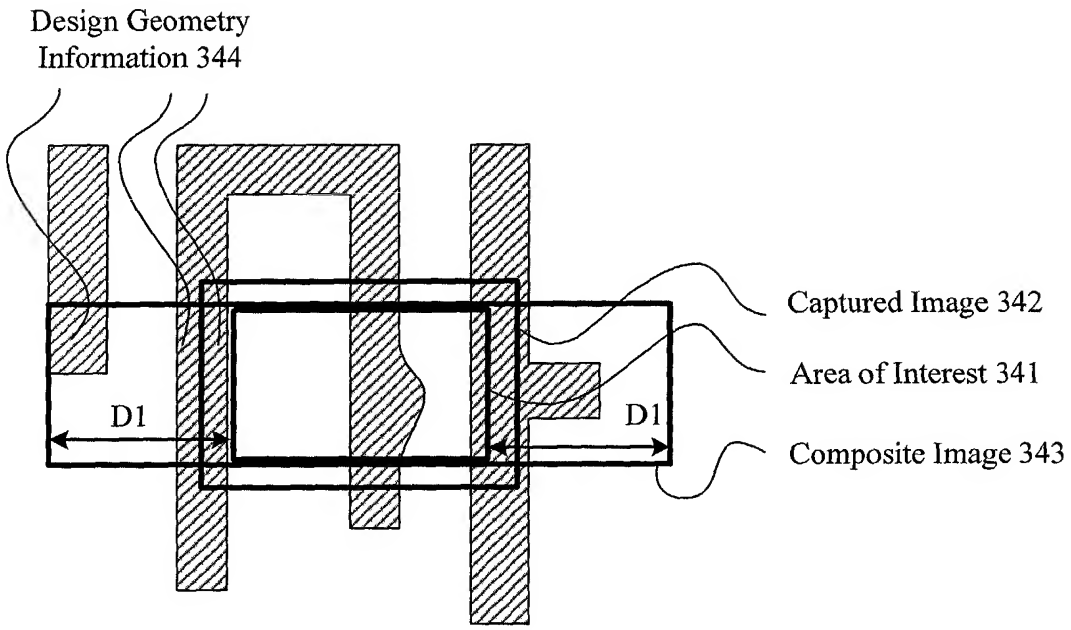

Figure 3E

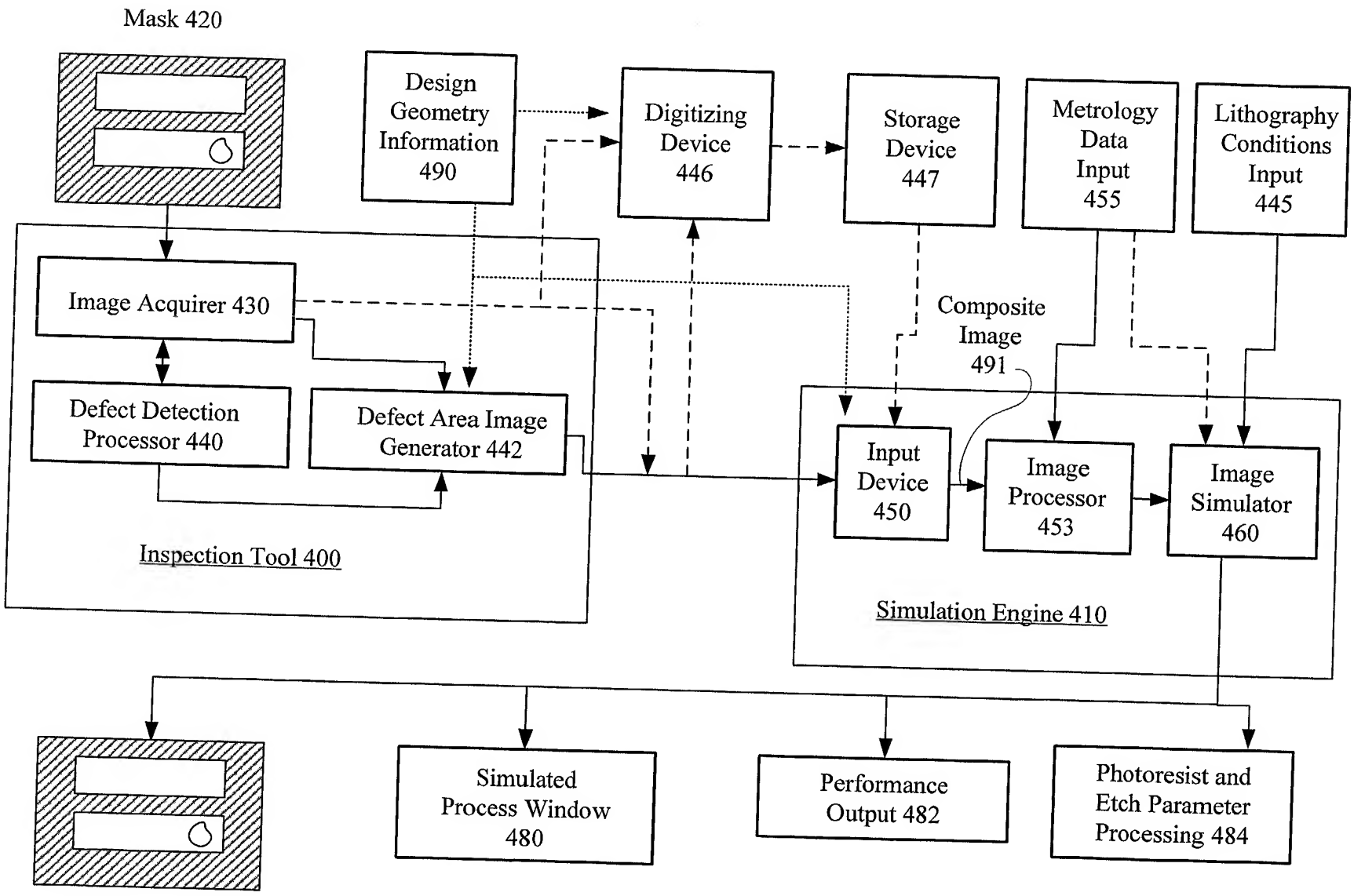
Mask 420
Design Geometry Information 490
Digitizing Device 446
Storage Device 447
Metrology Data Input 455
Lithography Conditions Input 445
Image Acquirer 430
Composite Image 491
Defect Detection Processor 440
Defect Area Image Generator 442
Input Device 450
Image Processor 453
Image Simulator 460
Inspection Tool 400
Simulation Engine 410
Simulated Process Window 480
Performance Output 482
Photoresist and Etch Parameter Processing 484
Simulated Wafer Image 470

Figure 4

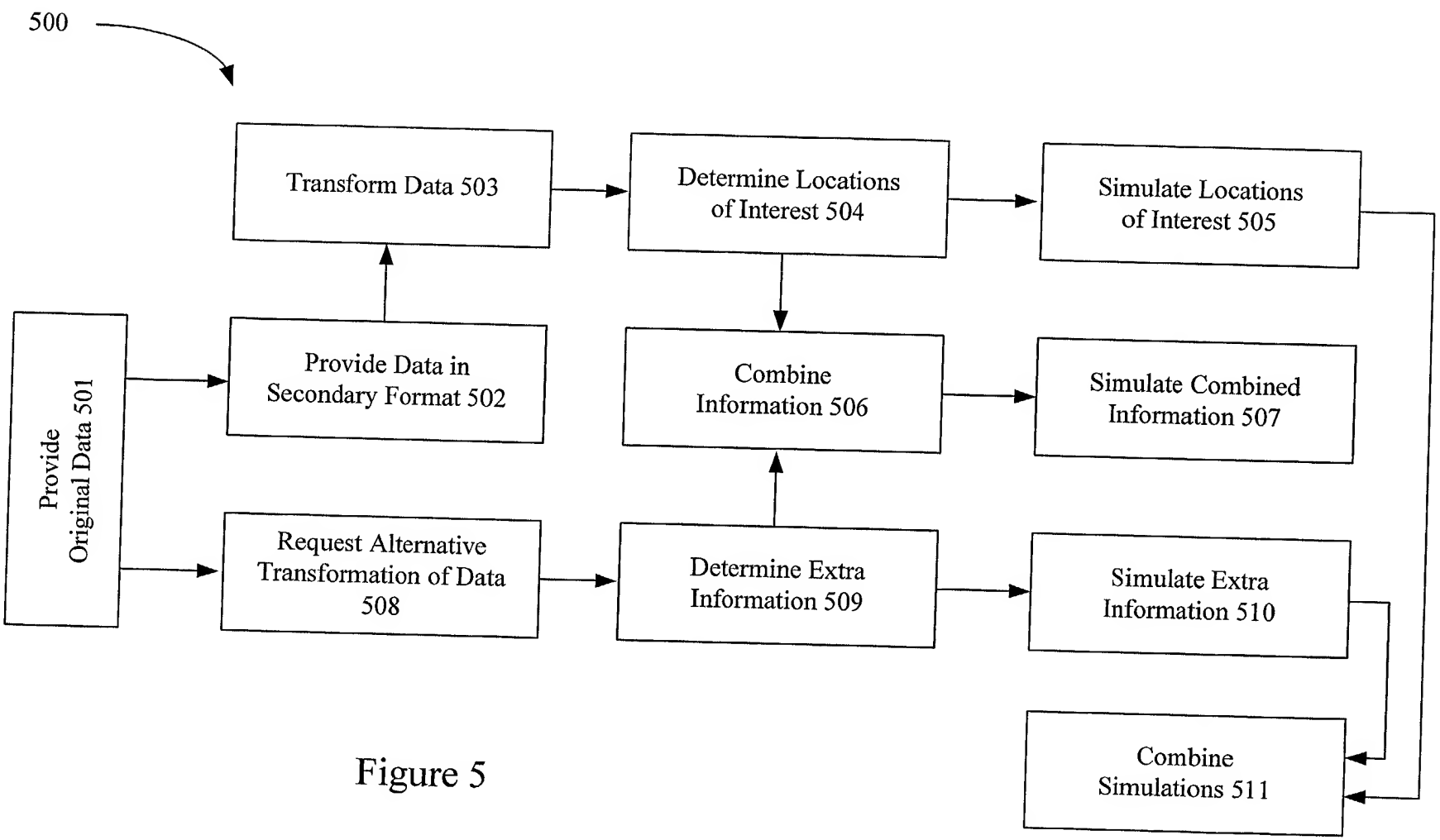
500
Transform Data 503
Determine Locations of Interest 504
Simulate Locations of Interest 505
Provide Original Data 501
Provide Data in Secondary Format 502
Combine Information 506
Simulate Combined Information 507
Request Alternative Transformation of Data 508
Determine Extra Information 509
Simulate Extra Information 510
Combine Simulations 511

Figure 5

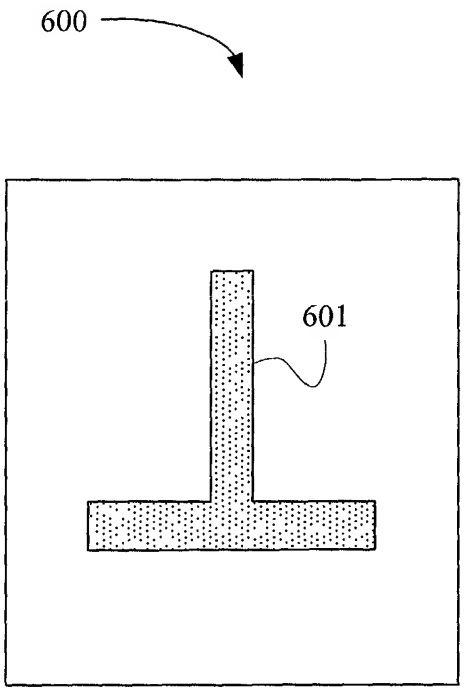

Figure 6A

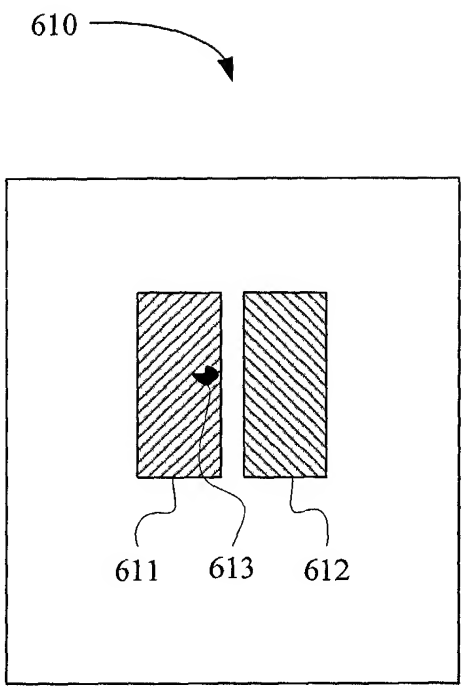

Figure 6B

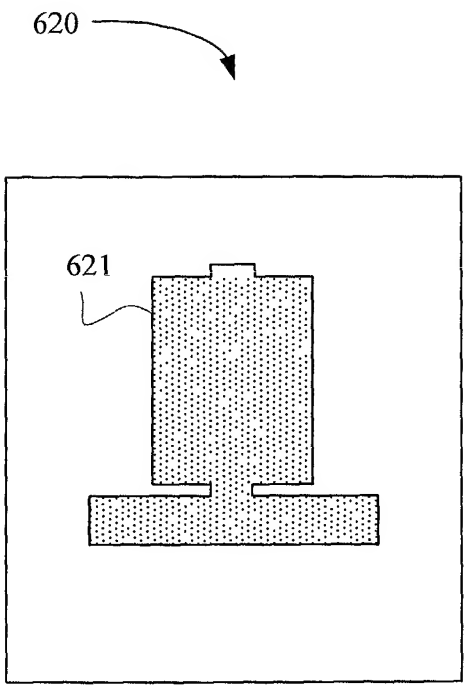

Figure 6C